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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,313	12/15/2003	Hee Bok Kang	40296-0055	8967

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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 10/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/734,313	KANG, HEE BOK	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *12-24* is/are withdrawn from consideration.

5)☒ Claim(s) *4-11* is/are allowed.

6)☒ Claim(s) *1-3 and 25-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/12/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

DETAILED ACTION

1. Claims 1-28 are pending in the application.

Election/Restrictions

2. Applicant's election without traverse of Group I in the reply filed on 21 July 2005 is acknowledged.

Claims 12-24 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Claims 25-28 are linking claims. Election was made **without** traverse in the reply filed on 21 July 2005. The restriction requirement is made final.

Information Disclosure Statement

3. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 12 May 2005. The information disclosed therein has been considered.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2 and 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizugaki et al. (U.S. Pat. Appl. Pub. No. 2002/0054523) in view of Sato (U.S. Pat. No. 4,195,238) and Mattausch (U.S. Pat. No. 6,141,287).

Regarding claims 1 and 2, Mizugaki, for example in Figs. 4-8, discloses a nonvolatile ferroelectric memory control device (see paragraph [0197] and [0198]) comprising: a page address buffer (included in 60 in Fig. 4) for decoding a page address (A0 and A1, via 422 in Fig. 7); a row address latch unit (34 in Fig. 8) for outputting a row address (A8-A19); an address transition detector for detecting transition of the row address (RATD 130), and for outputting an address transition detecting signal (RAT); and a chip control signal generator (for example, 42 in Fig. 6) for selectively generating a control signal (#EX0) to control a chip operation (via 38 in Fig. 8) in response to the address transition detecting signal (RAT).

Mizugaki does not disclose that the page address is latched in response to the chip enable signal, that the page address has a block page address region and a column page address region, and that the latched row address is detected by the address transition detector.

Sato, for example in Figs. 1, 4 and 5, discloses an address buffer that latches an address (via, for example, a latch comprising Q2-Q5) in response to a chip enable signal (CE).

Mattausch, for example in Fig. 2, discloses a page address (A12...AN2) having a block page address region (for selecting one row of pages or blocks SB2 via RAG) and a column page address region (for selecting a column from a selected row of pages or blocks SB2 via SAG).

Since an address buffer that latches an address in response to a chip enable signal was common and well known in the art (as exemplified in Sato), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to latch the address A0-

A19 in response to a chip enable signal in the address buffer of Mizugaki, such that the latched row address would be detected by the address transition detector 130 of Mizugaki, for the purpose of reliably capturing the inputted address (see also Sato column 2, lines 3-7).

Further, since a multilevel-hierarchy memory architecture for a large capacity memory with a page address having a block page address region (or a block row address) and a column page address region (or a block column address) was common and well known in the art (as exemplified in Mattausch), and since Mizugaki also discloses different levels of memory hierarchies (see for example paragraph [0193]), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the arrangement of Mizugaki's memory to include a multilevel hierarchy, such that the page address would have a block page address region and a column page address region (as in Mattausch), for the purpose of efficiently accessing a large capacity ferroelectric memory (see for example Mattausch column 1, line 57 through column 2, line 3) and reducing power consumption associated with word line activation in such large capacity memory (see for example Mizugaki paragraph [0007]).

Regarding claims 25 and 26, the above Mizugaki/Sato/Mattausch combination further discloses, in Fig. 2 of Mattausch, a plurality of unit blocks (for example, each row of SB2 as a unit block), each unit block comprising a plurality of cell arrays (SBM1 within each SB2), a plurality of row decoders (WLD in each SB2) and a plurality of column pages (for example, each SB2 in a row block as a column page), wherein the plurality of column pages in one unit block constitutes a unit block page to be activated simultaneously (as implied in column 2, lines 59-67;

or accessing a row of SB2 is reasonable broadly interpreted as simultaneously activating the unit block page).

Regarding claims 27 and 28, the above Mizugaki/Sato/Mattausch combination further discloses, in Fig. 2 of Mattausch, a plurality of unit blocks (for example, each row of SB1 as a unit block) comprising a plurality of cell arrays (SB1); a common data bus unit for exchanging input/output data with the plurality of unit blocks (including PAP); a unit block page (for example, a row of SB2) comprising a plurality of column pages (SB2); and a data bus unit for exchanging input/output data with the unit block page (including IOP), wherein the plurality of column pages in the unit block page are activated simultaneously (as implied in column 2, lines 59-67; or accessing a row of SB2 is reasonable broadly interpreted as simultaneously activating the unit block page).

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizugaki et al. in view of Sato and Mattausch as applied to claim 1 above, and further in view of Kozaru et al. (U.S. Pat. No. 5,991,223).

Regarding claim 3, the above Mizugaki/Sato/Mattausch combination discloses a device as in claim 1, and Mizugaki further discloses that the row address is arranged in more significant bit region (A8-A19 in Fig. 4), with the exception of a column page address of the page address arranged in less significant bit region, and a block page address of the page address arranged between the row address region and the column page address region.

Kozaro, for example in Fig. 2, discloses alternate address arrangements for different address regions (for example, the row address in the middle region and rearranging address regions).

Since various arrangements of address regions were common and well known in the art (as exemplified in Kozaro and Mizugaki), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to rearrange the page address regions of the Mizugaki/Sato/ Mattausch combination, such that a column page address of the page address is arranged in less significant bit region and a block page address of the page address is arranged between the row address region and the column page address region, for the purpose of providing an optimum arrangement of the page address regions.

Allowable Subject Matter

7. Claims 4-11 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 4, the prior arts of record do not disclose or suggest a nonvolatile ferroelectric memory control device as recited in claim 4, and particularly, a synthesizer for outputting a transition synthesizing signal in response to the address transition detecting signal, the reset transition detecting signal and the write enable transition detecting signal (in a memory with a page address having a block page address region and a column page address).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

10/3/05

Jung (John) Hur
Patent Examiner
Art Unit 2824

jhh